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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,180	03/01/2004	David E. Freker	42P18616	3194

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EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 08/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,180	FREKER ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 11 is objected to because of the following informalities: "ting" should be "adjusting". Appropriate correction is required.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 15-17 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. "Machine-accessible medium" includes propagated signals [pg.6 of original specification] that is non-statutory as not being tangibly embodied in a manner so as to be executable and is non-statutory for failing to be in one of the categories of invention.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-2, 4-5, 7-9, 12-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Zumkehr, US Publication 20030005346.

6. In re claim 1, Zumkehr discloses an apparatus [fig.1] comprising:

- A plurality of slave delay lock loops (DLLs) [210] in a memory interface [40] to adjust timing between a plurality of signals [100] to compensate for timing skew [center to avoid setup/hold time] [fig.3; 0003].

- A plurality of input/output (I/O) buffers [310] to output the plurality of signals to one or more memory devices [flops] coupled to the memory interface after adjusting the timing [fig.4].

7. As to claim 2, Zumkehr discloses, comprising a plurality of programmable configuration bits [220], coupled to the plurality of slave DLLs, to set an amount of delay each of the plurality of slave DLLs applies to one of the plurality of signals [0012, 0031; signals embodied as digital signals].

8. As to claim 4, Zumkehr discloses, comprising a master DLL [200], coupled to the plurality of slave DLLs, to calibrate the plurality of slave DLLs [0021].

9. As to claim 5, Zumkehr discloses, comprising a plurality of multiplexers [300] to couple each of the plurality of slave DLLs to one or more of the plurality of I/O buffers [fig.4].

10. As to claims 7 and 14, Zumkehr discloses, wherein the plurality of signals includes a plurality of memory control signals [100] [0019; controls latching].

11. In re claim 8, Zumkehr discloses a method comprising adjusting timing between a plurality of signals [100] using a plurality of slave delay lock loops (DLLs) [210] in a memory interface [40] before sending the signals to one or more memory devices [flops] [timing adjusted before latching] and sending the plurality of signals to the one or more memory devices [fig.3, 4; 0003].

12. As to claim 9, Zumkehr discloses, wherein adjusting the timing comprises: programming a plurality of configuration bits [220] to set an amount of delay each of the plurality of slave DLLs applies to one of the plurality of signals, the plurality of configuration bits being coupled to the plurality of slave DLLs [0012, 0031; signals embodied as digital signals].

13. As to claim 12, Zumkehr discloses, comprising calibrating the plurality of slave DLLs using a master DLL [200] [0021].

14. As to claim 13, Zumkehr discloses, comprising clocking each of a plurality of input/output (I/O) buffers [310] to output the plurality of signals in response to the amount of delay each of the plurality of slave DLLs applies to one of the plurality of signals [0024-25].

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 3, 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zumkehr as applied to claims 2 and 9above, and further in view of Adkisson, US Publication 20040225910.

17. Zumkehr taught each and every limitation of the claim as discussed above. Zumkehr discloses the amount of delay each of the slave DLLs applied to one of the plurality of signals to generate a memory clock signal [220]. Zumkehr did not disclose adjusting timing of a core clock signal in response to the amount of delay each of the slave DLLs applied to one of the plurality of signals to generate a memory clock signal.

18. Adkisson discloses adjusting timing of a core clock signal in response to the amount of delay applied to one of the plurality of signals to generate another clock signal [analogous to memory of Zumkehr] [0030].

19. It would have been obvious to one of ordinary skill in the art, having the teachings of Zumkehr and Adkisson before him at the time the invention was made, to modify the system taught by Zumkehr to include the adjusting of core clock taught by Adkisson, in order to synchronize the core clock with the other signals for proper operation [e.g., DQS]. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to alleviate synchronization problems such as skews [Adkisson: 0030].

20. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zumkehr as applied to claim 1 above, and further in view of Keeth et al., US Patent 6687185, hereinafter Keeth.

21. Zumkehr taught each and every limitation of the claim as discussed above. Zumkehr did not disclose clock trees.

22. Keeth discloses a plurality of clock trees [133], each of the plurality of clock trees having a root coupled to an output of each of the plurality of slave DLLs [132], to clock each of the plurality of I/O buffers [e.g., 124] [col.3, ll.38-56].

23. It would have been obvious to one of ordinary skill in the art, having the teachings of Zumkehr and Keeth before him at the time the invention was made, to modify the apparatus taught by Zumkehr to include the clock tree taught by Keeth, in order to obtain the claimed apparatus. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to alleviate effects related to PVT or other timing variations [Keeth: col.3, ll.38-56].

24. Claims 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zumkehr as applied to claim 1 above, and further in view of Wyatt, US Patent 6891543.

25. Zumkehr taught each and every limitation of the claim as discussed above. Zumekehr further discloses a system [fig.1] comprising a plurality of memory devices [flops] and a memory controller [40] coupled to the plurality of memory devices, the memory controller having a memory interface [part of 40]. Zumkehr did not disclose explicitly a graphics chip.

26. In re claim 18, Wyatt discloses a system comprising a graphics chip and a memory controller [interface engine] coupled to the plurality of memory device and the graphics chip [col.9, l.49 – col.10, l.3].

27. It would have been obvious to one of ordinary skill in the art, having the teachings of Zumkehr and Wyatt before him at the time the invention was made, to modify the system taught by Zumkehr to include the graphics chip taught by Wyatt, as graphics chips are very well known in the art and suitable for use in the system of Zumkehr. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to optimize processing [Wyatt: col.9, l.49 – col.10, l.3].

28. As to claim 19, Zumkehr discloses each and every limitation as discussed above in reference to claim 7.

29. As to claim 20, Zumkehr discloses each and every limitation as discussed above in reference to claim 4.

30. As to claim 21, Zumkehr discloses, comprising a processor [10] coupled to the memory controller.

31. As to claim 22, Zumkehr discloses, wherein the plurality of memory devices includes a plurality of double-data rate (DDR) dynamic random access memory (DRAM) devices [0003].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
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Tse Chen
August 18, 2006